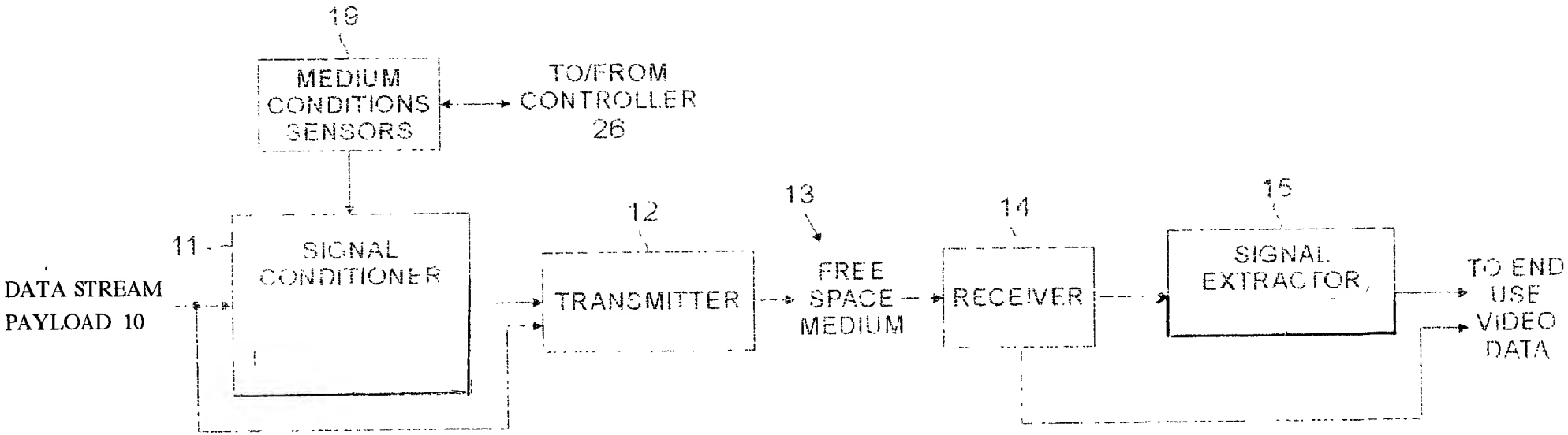

19
MEDIUM CONDITIONS SENSORS
TO/FROM CONTROLLER 26
11
SIGNAL CONDITIONER
DATA STREAM PAYLOAD 10
12
TRANSMITTER
13
FREE SPACE MEDIUM
14
RECEIVER
15
SIGNAL EXTRACTOR
TO END USE VIDEO DATA

FIG. 1

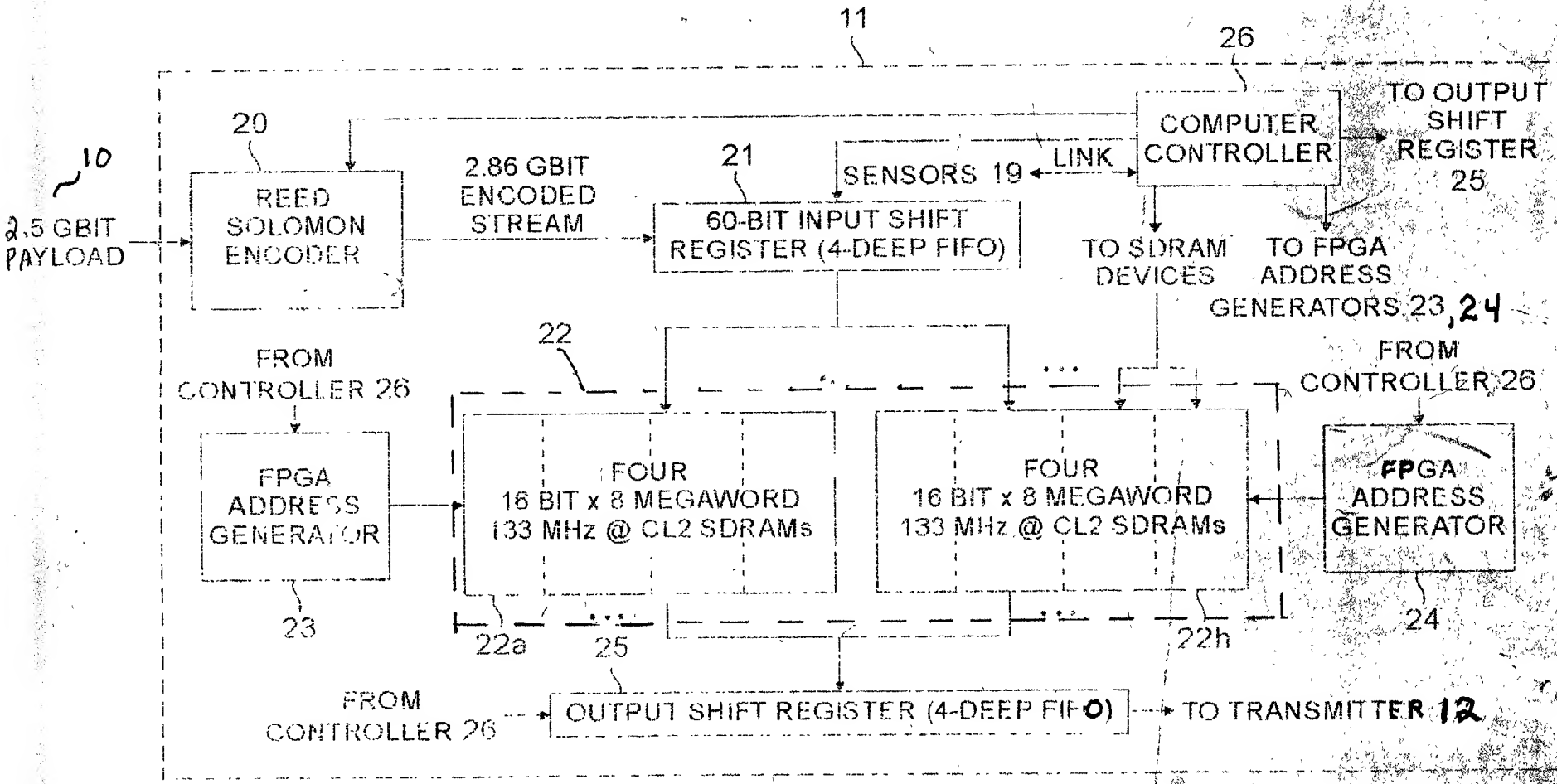
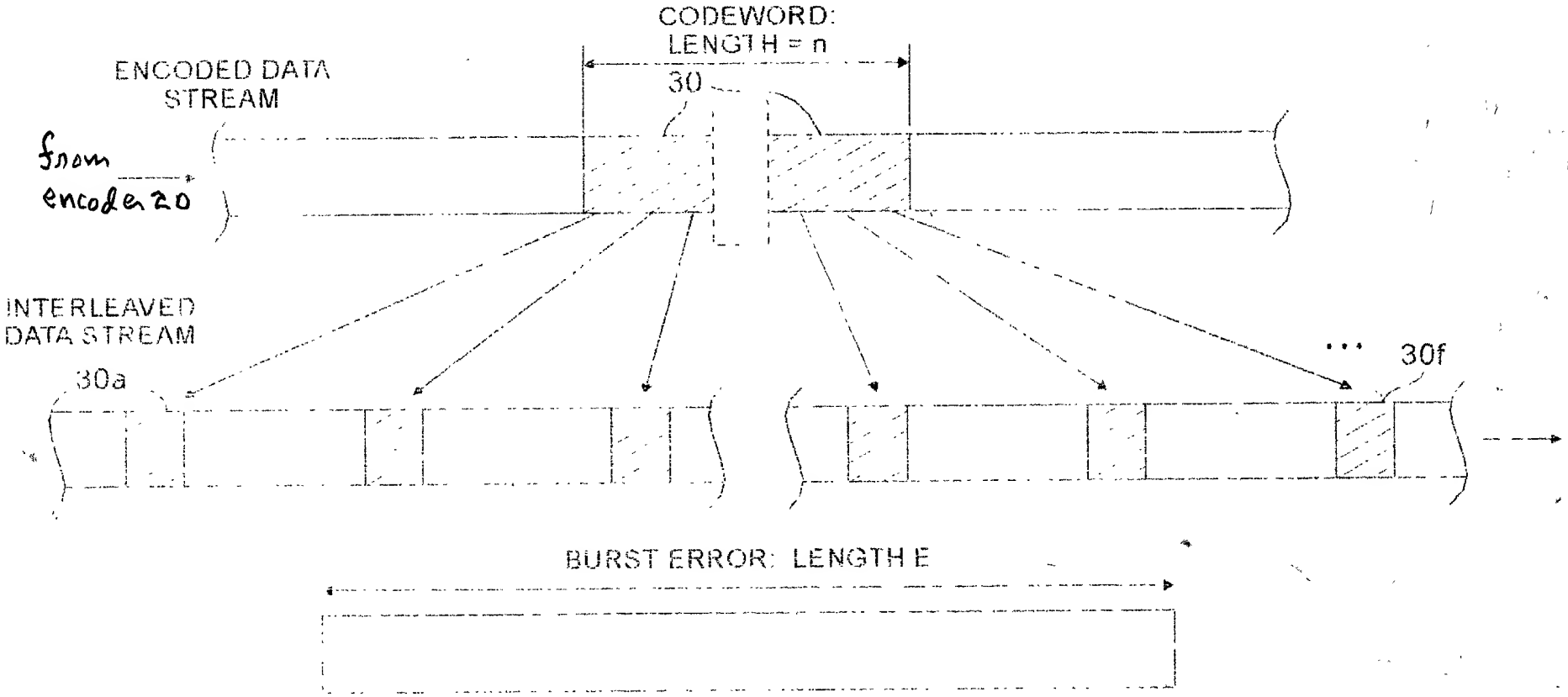

11
26
20
10
2.5 GBIT PAYLOAD
REED SOLOMON ENCODER
2.86 GBIT ENCODED STREAM
21
60-BIT INPUT SHIFT REGISTER (4-DEEP FIFO)
SENSORS 19
LINK
COMPUTER CONTROLLER
TO OUTPUT SHIFT REGISTER 25
TO SDRAM DEVICES
TO FPGA ADDRESS GENERATORS 23, 24
22
FROM CONTROLLER 26
FROM CONTROLLER 26
FPGA ADDRESS GENERATOR
FOUR 16 BIT x 8 MEGAWORD 133 MHz @ CL2 SDRAMs
FOUR 16 BIT x 8 MEGAWORD 133 MHz @ CL2 SDRAMs
FPGA ADDRESS GENERATOR
23
22a
25
22h
24
FROM CONTROLLER 26
OUTPUT SHIFT REGISTER (4-DEEP FIFO)
TO TRANSMITTER 12

FIG. 2



INTERLEAVING THE ENCODED PAYLOAD

FIG. 3

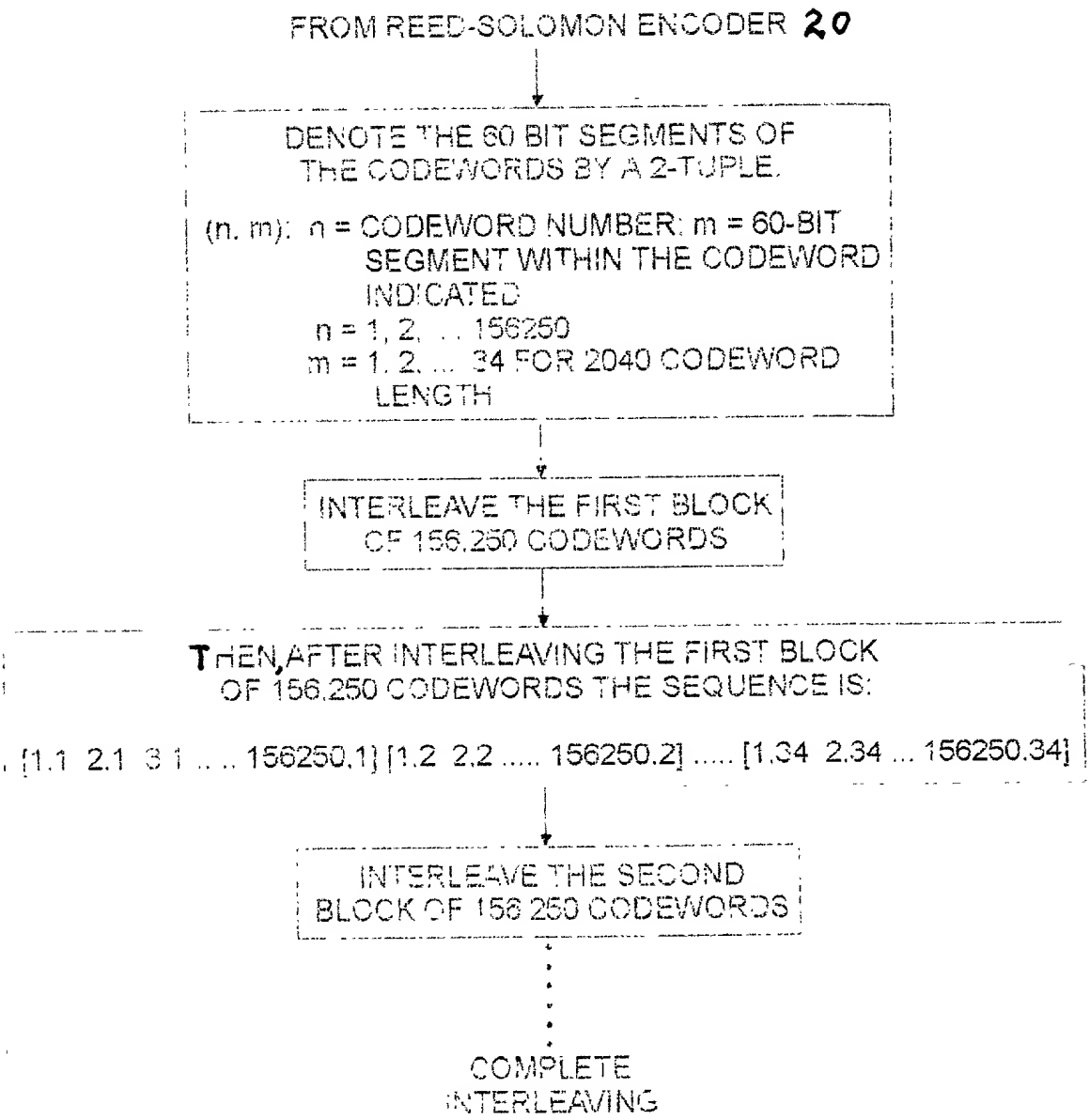

FROM REED-SOLOMON ENCODER 20
DENOTE THE 60 BIT SEGMENTS OF THE CODEWORDS BY A 2-TUPLE.
(n, m): n = CODEWORD NUMBER; m = 60-BIT SEGMENT WITHIN THE CODEWORD INDICATED
n = 1, 2, . . . 156250
m = 1, 2, ... 34 FOR 2040 CODEWORD LENGTH
INTERLEAVE THE FIRST BLOCK OF 156,250 CODEWORDS
THEN, AFTER INTERLEAVING THE FIRST BLOCK OF 156,250 CODEWORDS THE SEQUENCE IS:
, [1.1 2.1 3.1 . . . 156250.1] [1.2 2.2 ..... 156250.2] ..... [1.34 2.34 ... 156250.34]
INTERLEAVE THE SECOND BLOCK OF 156,250 CODEWORDS
COMPLETE INTERLEAVING

FIG. 4

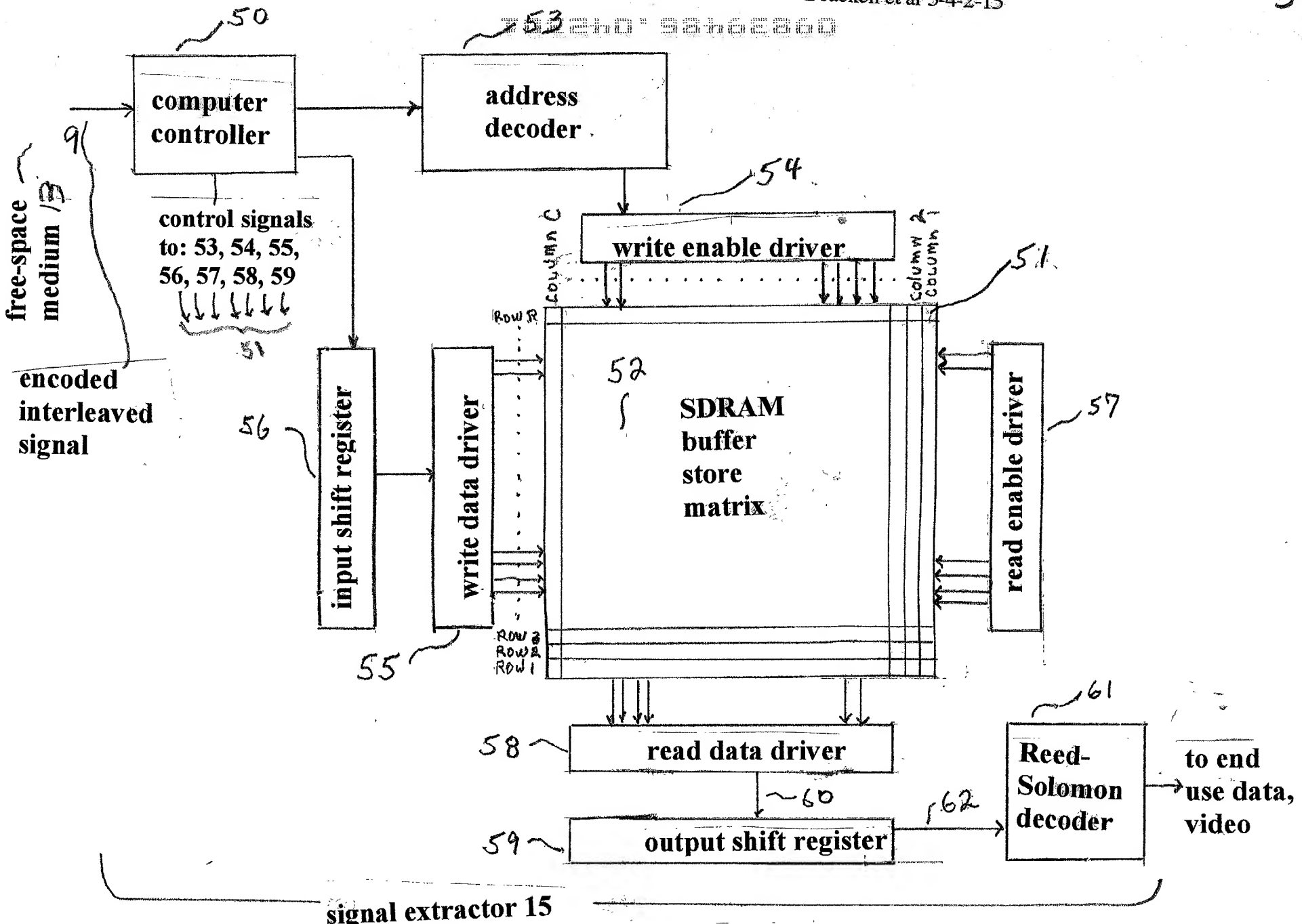

50
computer controller
53
address decoder
54
write enable driver
control signals to: 53, 54, 55, 56, 57, 58, 59
51
free-space medium 13
encoded interleaved signal
56
input shift register
write data driver
55
52
SDRAM buffer store matrix
read enable driver
57
Column C
Column 2
Row R
Row 3
Row 2
Row 1
58
read data driver
60
59
output shift register
62
61
Reed-Solomon decoder
to end use data, video
signal extractor 15

Fig. 5

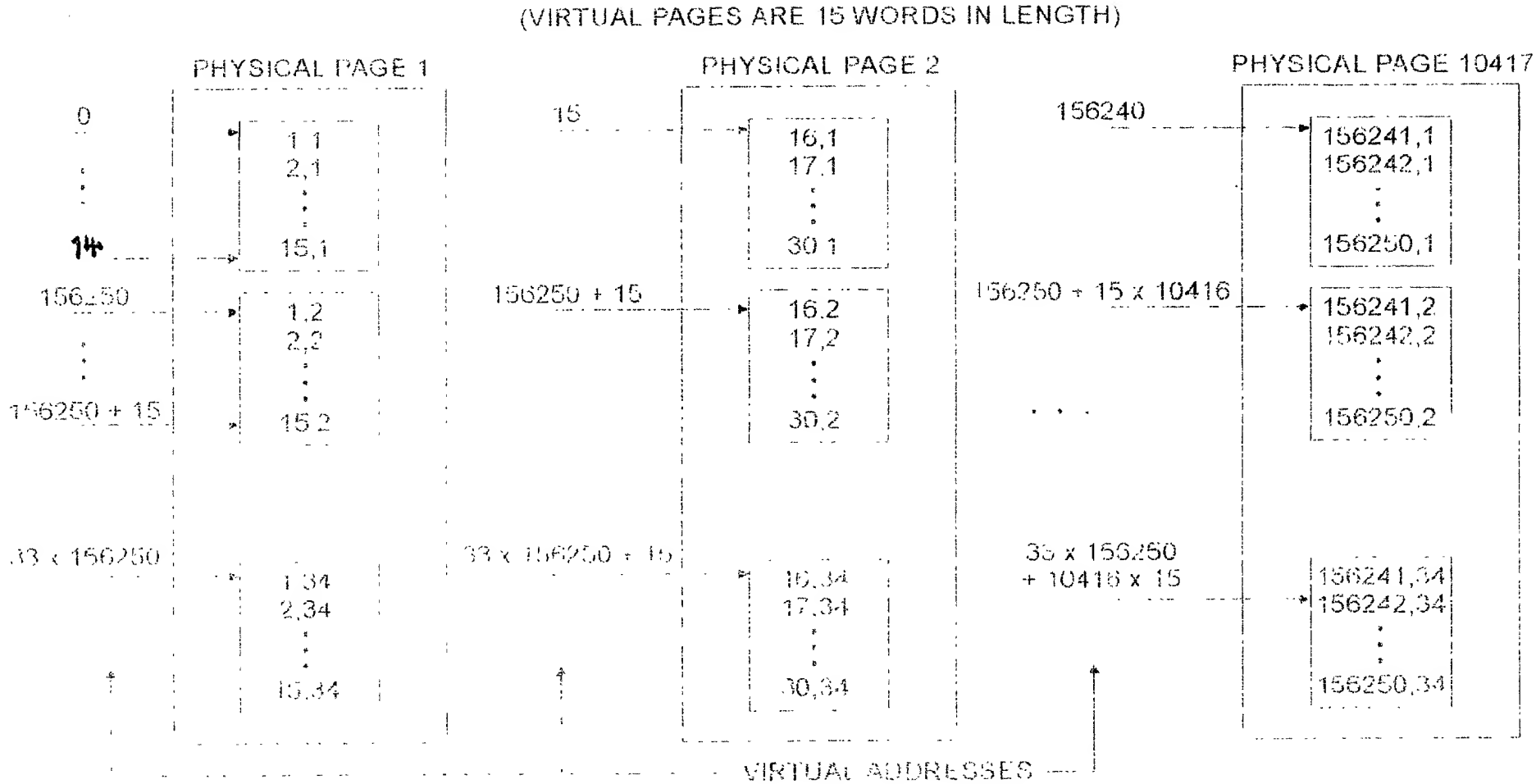

(VIRTUAL PAGES ARE 15 WORDS IN LENGTH)
PHYSICAL PAGE 1
PHYSICAL PAGE 2
PHYSICAL PAGE 10417
0
14
156250
156250 + 15
33 x 156250
15
156250 + 15
33 x 156250 + 15
156240
156250 + 15 x 10416
35 x 156250
+ 10416 x 15
1,1
2,1
15,1
1,2
2,2
15,2
1,34
2,34
15,34
16,1
17,1
30,1
16,2
17,2
30,2
16,34
17,34
30,34
156241,1
156242,1
156250,1
156241,2
156242,2
156250,2
156241,34
156242,34
156250,34
VIRTUAL ADDRESSES
REMAPPING ADDRESSES TO BALANCE
'READ' VS 'WRITE' OVERHEAD IN TERMS
OF SDRAM PAGE CHANGES

FIG. 6A

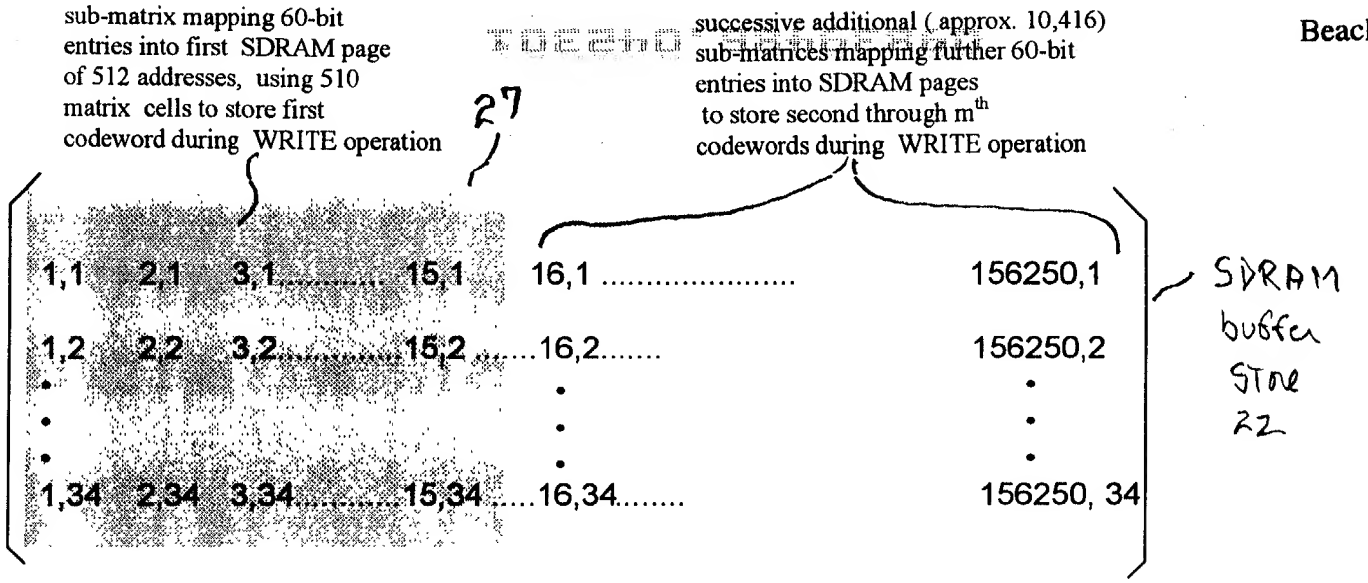


Fig. 6B :Codeword Segments Expressed as a Matrix

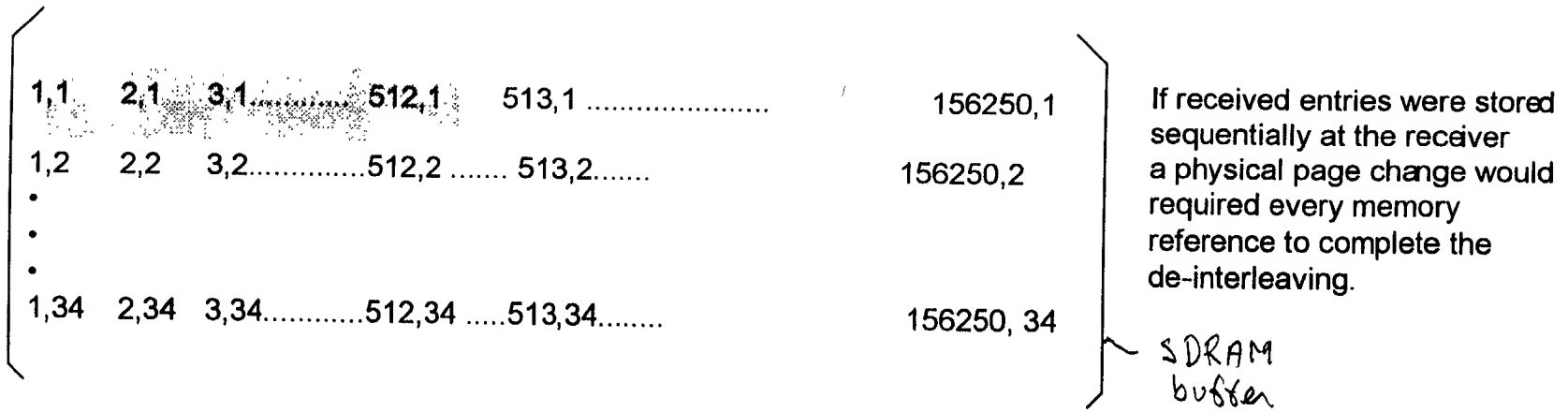


Fig. 6C : Shaded submatrix indicates segment of Received Matrix that Would be Held on One 512 Address page if Receiver Stored Entries Sequentially

Fig. 7A FLOW CHART OF PROCESS AT TRANSMITTER END

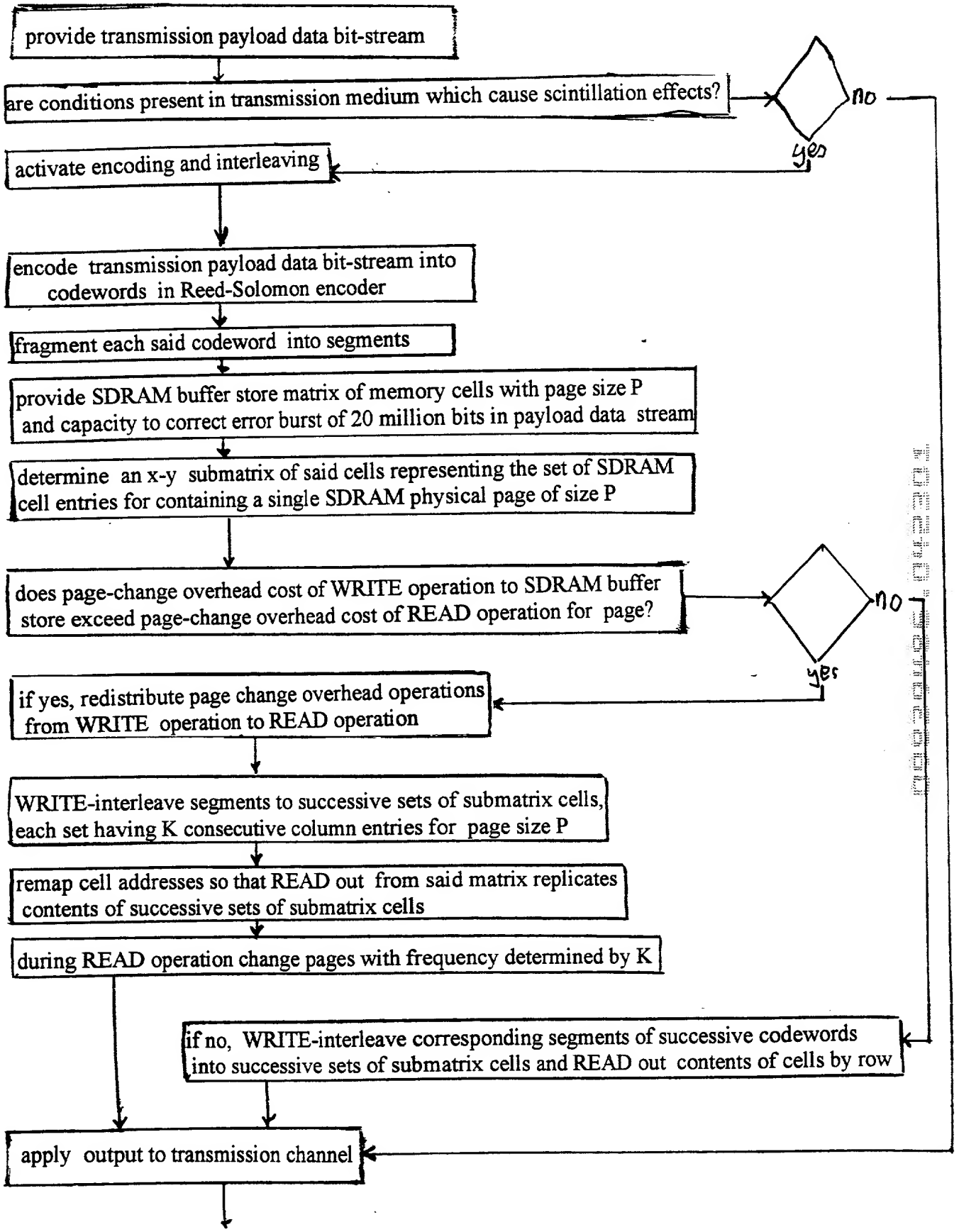
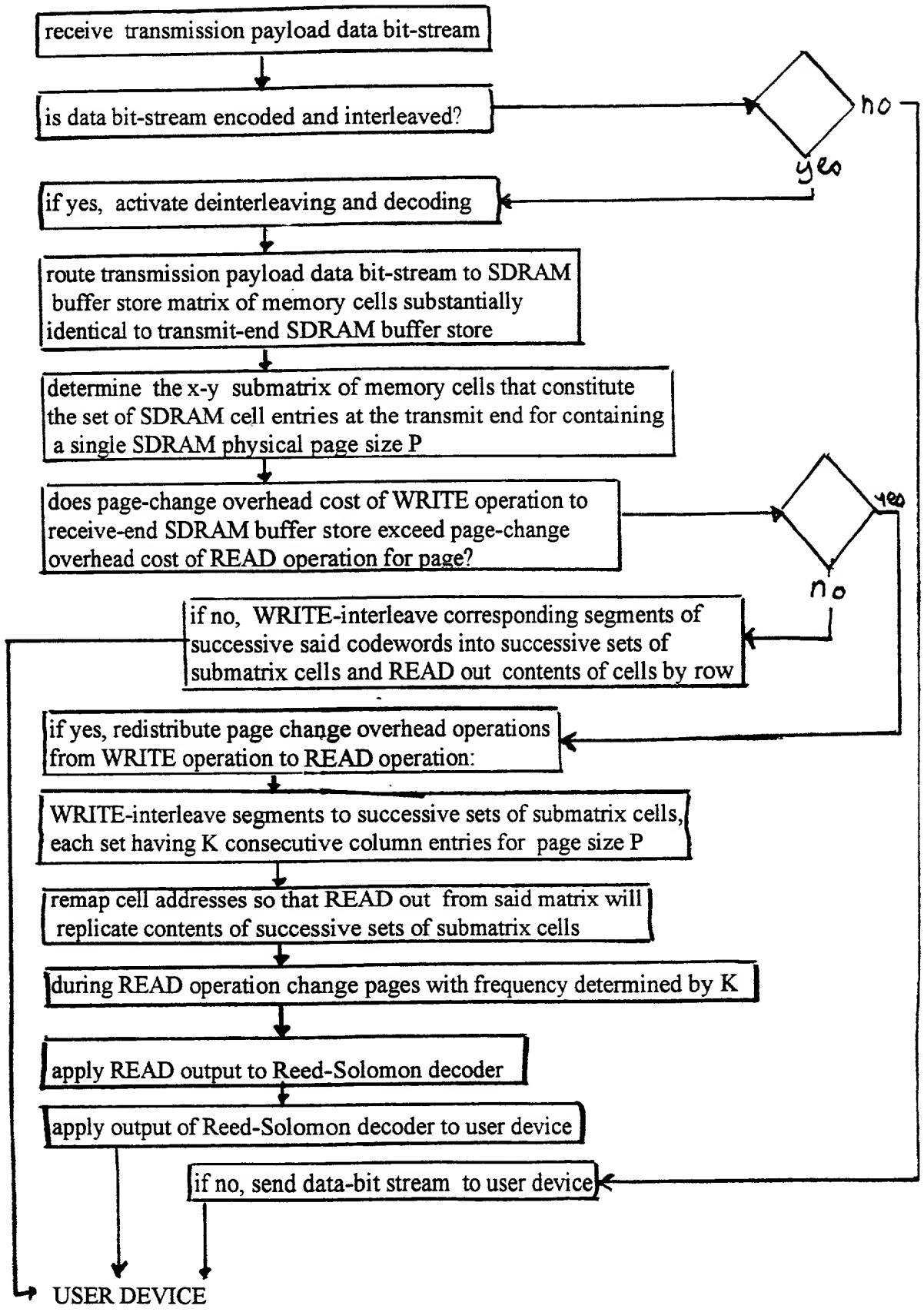


Fig. 7B FLOW CHART OF PROCESS AT RECEIVER END



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